M4050 SERIES

DC/DC POWER SUPPLY

PRODUCT HIGHLIGHTS

- **3U, 0.8 PITCH, VITA 62 COMPLIANT**
- **FAST INITIALIZATION TIME**
- **5 OUTPUTS**
- **OPTIONAL EXTENSION FOR HOLDUP CARD**
- **150W**

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Electrical Specifications

DC Input
16 to 36 V_{DC}
Max Non-Operating 100V
Options:
1) MIL-STD-704 (A-F) Normal and Abnormal Steady State
2) MIL-STD-704(A-F) transients Up to 50V, 80V
3) MIL-STD-1275 100V Surge

DC Output
VS1: 12V/2A
VS2: 3.3V/15A
VS3: 5V/12A
3.3V_Aux: 3.3V/1A
-12V_Aux: 12V/1A

Isolation
500V between Input and Output
500V between Input and Case 500V between Output and Case

Line/Load regulation
Less than 1% for 12V & 5V
Outputs 1.5% for 3.3V outputs
(No load to full load, –55°C to 90°C)

Efficiency
Up to 85 %
(Full load room temperature)

EMC
Complies with MIL-STD-461F (5µH LISN): CE101, CE102, CS101, CS114, CS115, CS116

Ripple and Noise
Typically less than 50mV_{p-p}(max. 1%$_p$). Measured across a 0.1µF capacitor and 10µF capacitor on load at input voltage of 18V-36V, across the whole temperature range.

Load Transient Overshoot and Undershoot
Output dynamic response of less than 5% at load Step of 30%-90%. Output returns to regulation in less than 1mSec

System Management
I2C/IPMI protocol available for voltages, currents and temperature for all voltages
(GAx, SCL, SDA)

Environmental [1]
Design to Meet MIL-STD-810G

Temperature
Operating: –55°C to +90°C at unit edge[1]
Storage: –55°C to +125°C

Altitude
Method 500.5, Procedure I & II
Storage/Air Transport: 40 kft
Operation/Air carriage: 70 kft

Salt Fog:
Method 509.5

Fungus
Does not support fungus growth, in accordance with the guidelines of MIL- STD-454, Requirement 4.

Humidity
Method 507.5, Up to 95% RH

Shock
Vita 47 Level ECC4

Vibration
Shock: Saw-tooth, 40g peak, 11mS.
Vibration: Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)

Reliability: 225,900 Hours, calculated IAW MIL-HDBK-217F Notice 2 at +45°C, AUC.

Note 1: 90°C at 50% Load

Protections [1]

Input

- **Inrush Current Limiter**
  Peak value of 5 x I_{IN} for initial inrush currents lasting more than 50µSec.
- **Under Voltage**
  Unit shuts down when input DC voltage drops below 15.3± 0.5V_{DC}.
  Automatic restart when input voltage returns to nominal range.
- **Over Voltage Lock-Out**
  Unit shuts down when input voltages rise above 55 ± 2V_{DC}.
  Automatic restart when input voltage returns to nominal range.

Output

- **Passive over voltage protection on Aux outputs**
  Transorb, selected at 25% ± 5% above nominal voltage, is placed across the output for passive voltage limit.
- **Active over voltage protection on VS# outputs**
  20% ± 5% above nominal voltage. Automatic recovery when output voltage drops below threshold.
- **Overload / Short-Circuit Protection**
  Continuous protection (10-30% above maximum current) for unlimited time (Hiccup).
  Automatic recovery when overload / short circuit removed.

General

- **Over Temperature Protection**
  Automatic shutdown at internal temperature of 95 ± 5°C.
  Automatic recovery when temperature drops below 90 ± 5°C.

Note 1: Thresholds and protections can be modified / removed – please consult factory)

Functions and Signals - According to VITA 62

Signal No.	Signal Name	Type	Description
1	FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs or Input line is under 17V. Normally Open, Low during failure.
2	SYSRESET*	Output	Indicates to other modules in the system that all outputs are within their working level. Normally Open, Low during failure.
3	INHIBIT*	Input	Combined with ENABLE, controls power supply outputs. Please refer to Table 1. Signal has Internal Pullup see picture 1. Do not tied the signal to unit 3.3V or 3.3VAux
4	ENABLE*	Input	Combined with INHIBT, controls power supply outputs. Please refer to Table 1. Signal has Internal Pullup see picture 1.
5	GA0*, GA1*	Input	Used for geographical addressing. GA1 is the most significant bit and GA0 is the least significant bit.
6	SCL, SDA	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared.
7	Alert Bit	Output	Open Drain output, goes low when Input voltage drops below 17V
8	VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
9	Signal RTN	Gnd	Signal ground for all signal. Internally tied to output Power ground

INHIBIT*	**Low**	**Low**	**High**	**High**
ENABLE*	**Low**	**High**	**Low**	**High**
Outputs Status	OFF	OFF	ON	OFF

Table 1: Inhibit & Enable functionality.

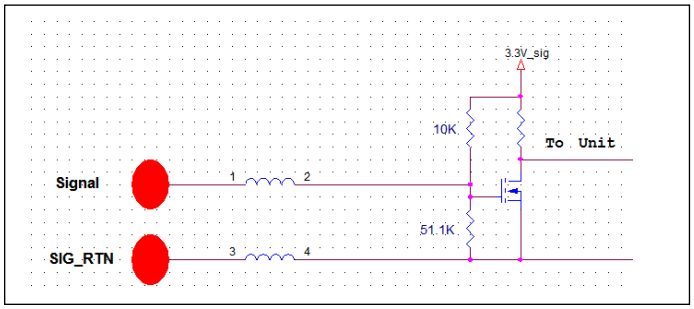
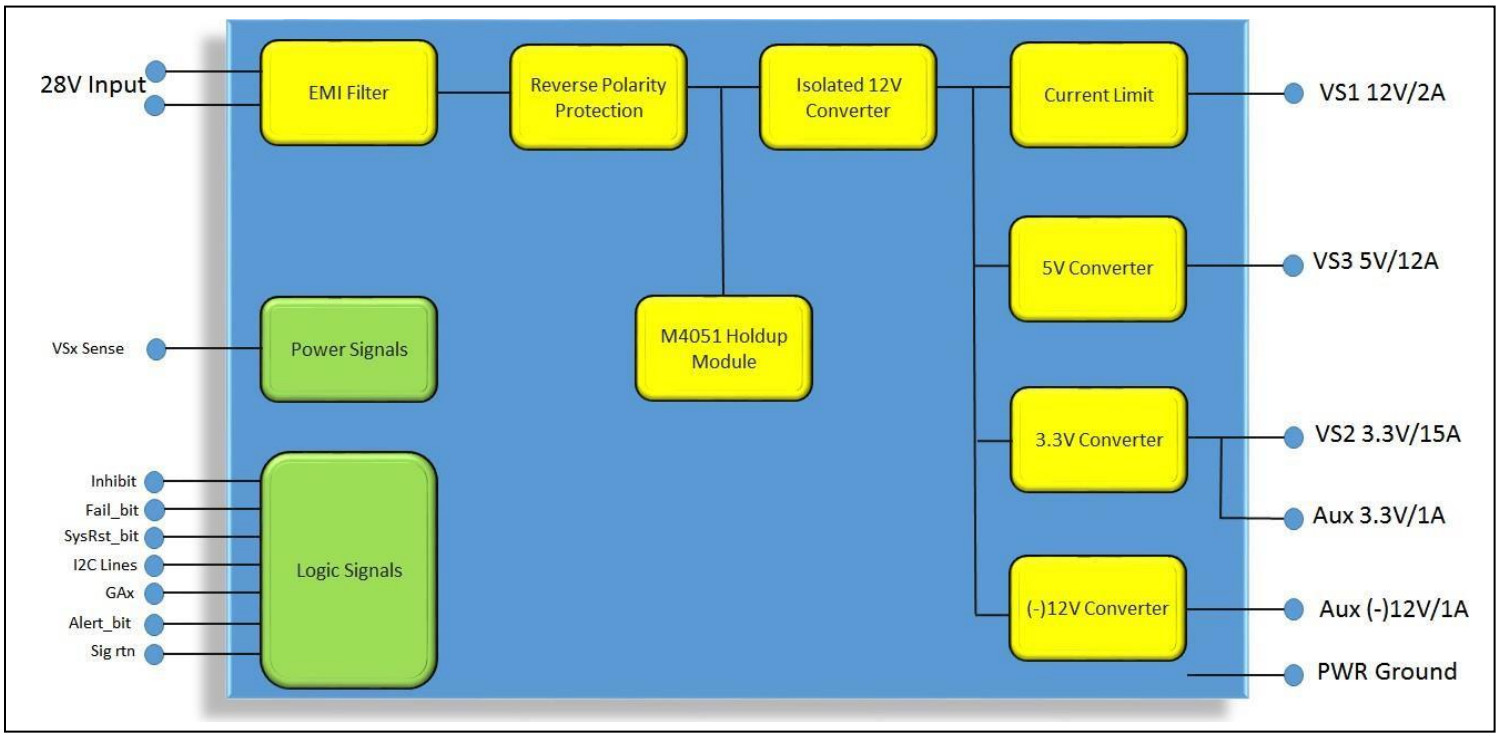


Figure 1: Inhibit & Enable Input Stage.

Simplified Block Diagram



Detailed Information

1. Input Voltage Operation.

The Power supply steady state operation voltage is 18V to 36V and will continuously work at input voltages up to 50V and down to 16V. During transients or surges above 50V or below 16V for more than 50uSec the unit will shut down. Automatic recovery occurs when input line drops down below 48V.

1.1 Low Line Turn-on and Turn-off Limits

To avoid turn-on and turn-off glitches, the unit has about 3.5V hysteresis. The turn-on threshold is under 20V and turn- off under 16V. These limits can be adjusted, contact factory for more information.

2. Outputs regulation

The unit contains accurate internal sense lines to keep output voltage at less than 1.5% regulation for all Line/ Load and temperature range (see Table 2).

Output	12V/2A	5V/12A	3.3V/15A	3.3VAux	12VAux	(-)12VAux/1A
Voltage Range	11.85 - 12.15	4.95 - 5.05	3.25 - 3.35	Follow 3.3V/15A	N/A	(-)11.85 - (-)12.15

Table 2: Single Unit

2.1.1. Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop.
Sense Lines proper connection is shown in Figure 2.
Each VSx output has its own *Sense Lines*, additional common *Sense RTN Line* is provided for all VSx Outputs (VITA 62 Standard).
Contact Factory for Sense configuration different than the VITA 62 Standard

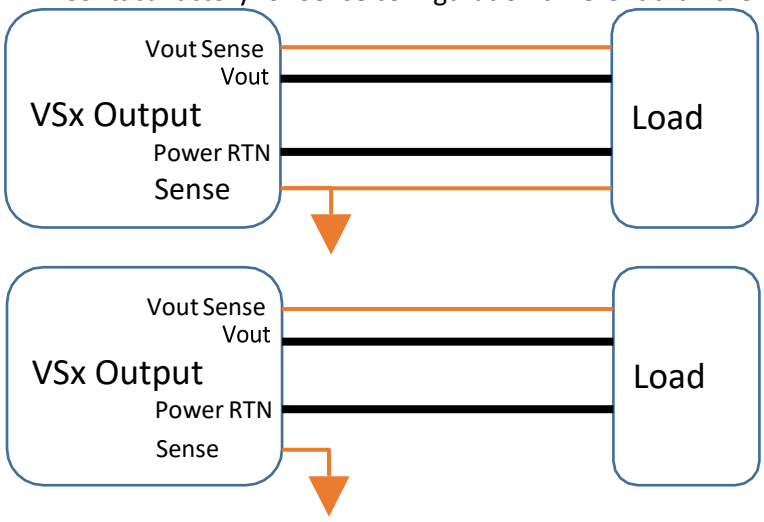


Figure 2: Sense line connection

3.0 Output Signals

All discrete signals are referred to Signal RTN.

3.1 FAIL*

*FAIL** – Indicates a failure in one of the Outputs or Input line is under 17V. Output which is turned off by *Enable* or
Inhibit, will not be considered as a Fail. Signal Normally Open.

3.2 SYSRESET*

*SYSRESET** – Indicates that all Outputs are in or above their nominal range. Signal Normally Open. See Figure 3.

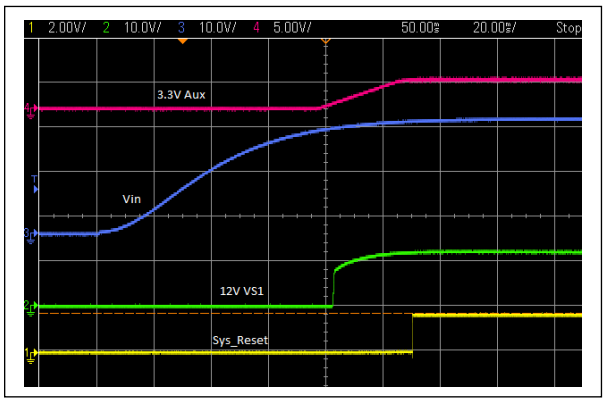


Figure 3

3.3 ALERT

ALERT – Indicates that Input voltage is under 17V, will go back high above 18V. Signal Normally Open.

4. I²C Protocol

I2C Software Version 1.2 – support I2C (IPMI protocol is optional)

Electrical Parameters

Vcc: 3.3VDC

Pull-up: 2.0kOhm Input capacitance: 330pf

Slave Device Addressing

- 16 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Address
- Support Slot Addressing per VITA 62
- Support Global Address 1010101 R/W

	MSB							LSB
Slot Number	A6	A5	A4	A3	A2	A1/*GA1	A0/*GA0	R/W
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	
Global Address	1	0	1	0	1	0	1	

* Slot location is determined by GAx per VITA 62.

Communications Supported

Single read sequence

S	Physical Address	W	A	Memory Address	A	S	Physical Address	R	A	DATA	A	P
	A6:A0	0	0	B7:B0	0		A6:A0	1	0	D7:D0	1	

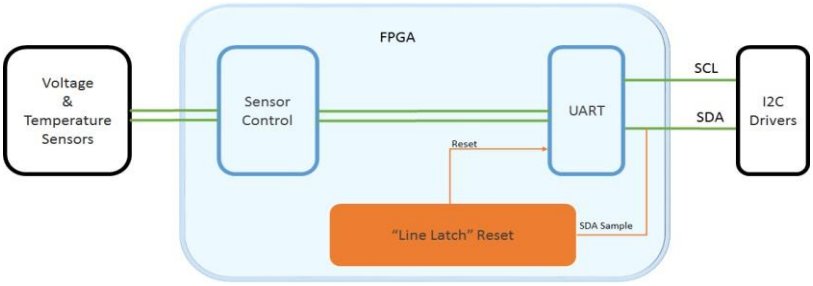
Sequential read sequence

S	Physical Address	W	A	Memory Address	A	S	Physical Address	R	A	DATA	A	DATA	A	• • •	DATA	A	P
	A6:A0	0	0	B7:B0	0		A6:A0	1	0	D7:D0	0	D7:D0	0		D7:D0	1	

S – Start, **P**- Stop
W – Write bit
A – Acknowledge by master
A – Acknowledge by slave, **DATA** – Slave response

SDA Timeout Reset

The Uart SDA Line is default “Open” unless data is transmitted by the slave. As a second level precaution the FPGA has a separate VHDL entity which sense the FPGA’s SDA Line and forced it open in case it detects a 150mSec duration of “Low” SDA Line. The line will be released back to normal once the entity will detect a new attempt of UART communication.

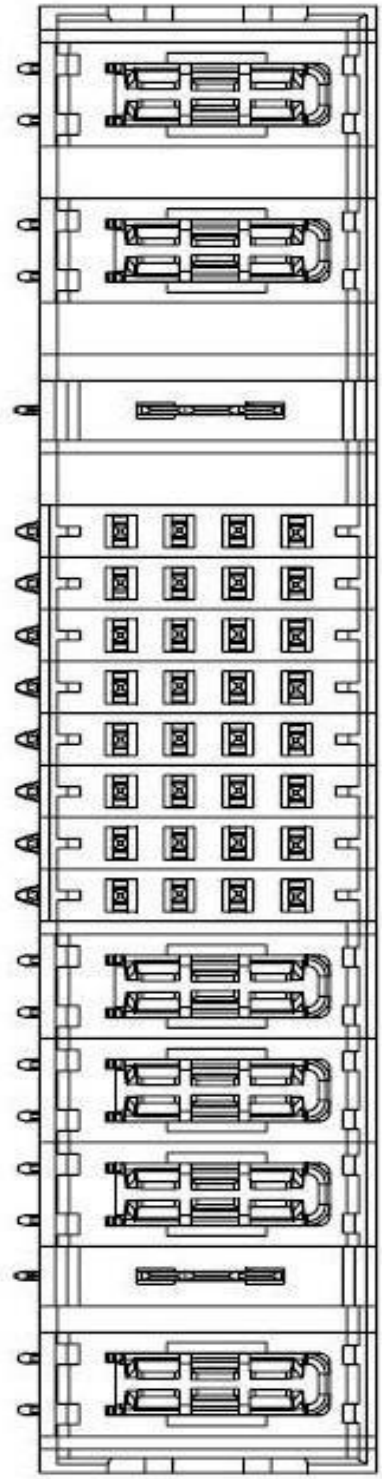


Memory

Byte #	Data Type	Meaning	Interpretation	Reading Range
0	S Integer, MSB First	Temperature	T(C°)=+/-7bit Dec Note1	-55 C° to 125 C°
1	U Integer, MSB First	Input Voltage	Not applicable	00 Hex
2	U Integer, MSB First	12V VS1 Voltage	V(out) = Data/ m2 Note2	0 to 20.48V
3	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data/ m2	0 to 20.48V
4	U Integer, MSB First	5V VS3 Voltage	V(out) = Data/ m2	0 to 20.48V
5	U Integer, MSB First	12V Aux Voltage	Not applicable	00 Hex
6	U Integer, MSB First	(-)12V Aux Voltage	V(out) =(-) Data/ m2	0 to 20.48V
7	U Integer, MSB First	3.3V Aux Voltage	V(out) = Data/ m2	0 to 20.48V
8	U Integer, MSB First	12V VS1 Current	Not applicable	00 Hex
9	U Integer, MSB First	3.3V VS2 Current	Not applicable	00 Hex
10	U Integer, MSB First	5V VS3 Current	Not applicable	00 Hex
11	Binary	Fail Bit & SysReset Bit	0000 , 00 Fail, SysReset Note5	00000,00xx
12-13	Character String(ASCII)	Unit version	Rev X,Y Note4	2 Characters
14-15	Character String(ASCII)	Firmware Version	Version A.B Note3	2 Characters
16-19	Character String(ASCII)	Part Number	4050	4 Characters

Note1: Temperature = Reading (Dec). MSB=’1’ for negative numbers.
Note2: m2= 20.48/255. Vout = (Reading / 255) * 20.48 [V]
Note3: Example: Firmware Version 2.3 32 Hex, 33 Hex
Note 4: Example: Unit Version 0A 30, 41
Note5: Fail & SysReset are the last two bits of the Byte 11. ‘1’ signal is good, ‘0’ signal Fail. “0000, 00 Fail Bit, SysReset Bit”

Pin Assignment

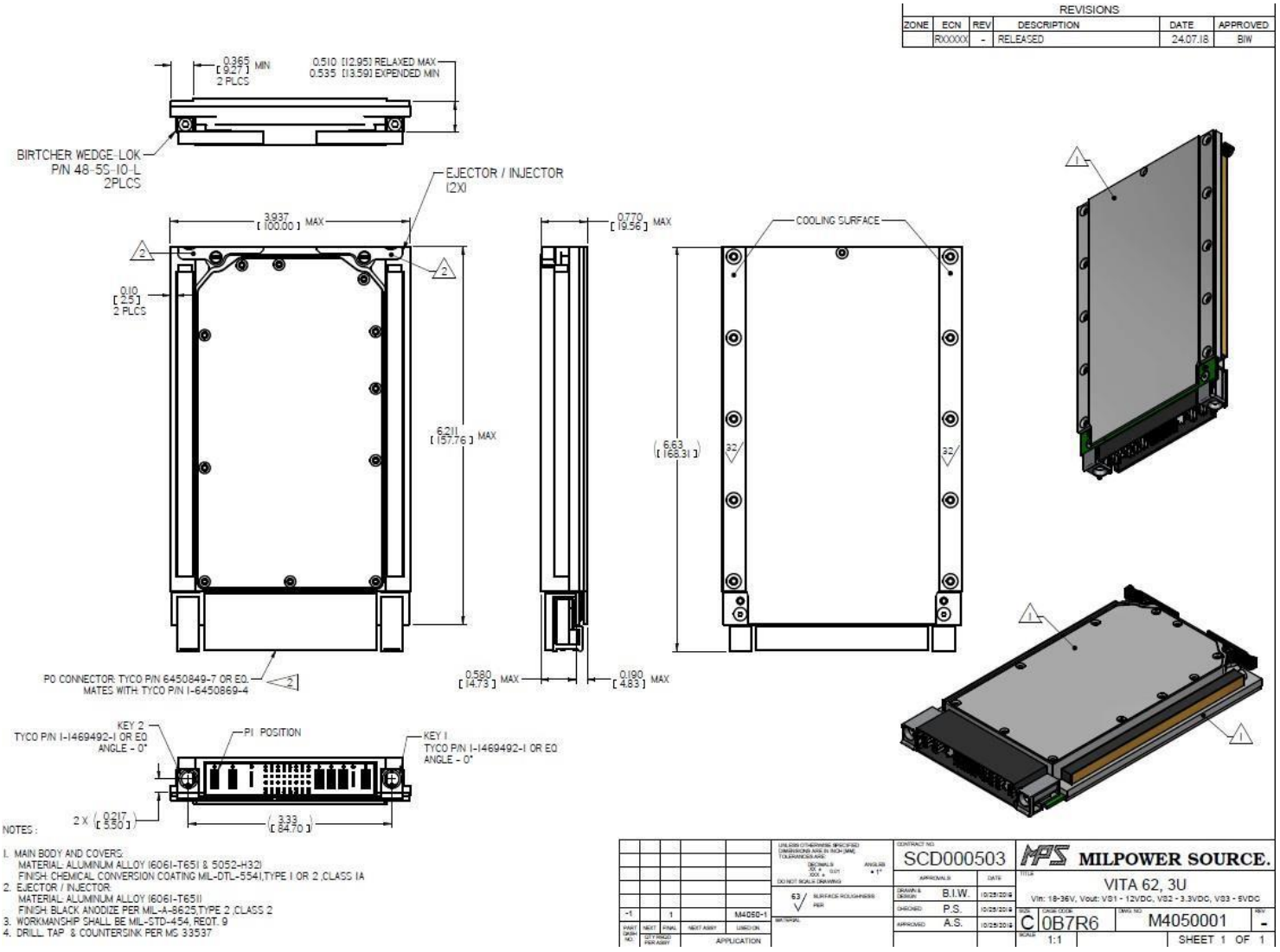


PART NUMBER	ROWS	POWER	SIGNAL								POWER				
		P1	LP1	1	2	3	4	5	6	7	8	P3	P4	P5	LP2	P6
6450849-7	D			Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5					
	C	TT	LT	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	TT	TT	TT	LT	TT
	B			R5	R5	R5	R5	R5	R5	R5	R5					
	A			O5	O5	O5	O5	O5	O5	O5	O1					
2ACP+1LP+32S+3HDP+1LP+1HDP																

Pin Assignment

Pin Number	*Pin Name*
P1	-DC_IN
P2	+DC_IN
LP1	CHASSIS
P3	VS3
P4	POWER_RETURN
P5	POWER_RETURN
LP2	VS2
P6	VS1
A8	VS1_SENSE
B8	VS2_SENSE
C8	VS3_SENSE
D8	SENSE_RETURN
A7	VS1_SHARE / N.C
B7	VS2_SHARE / N.C
C7	VS3_SHARE / N.C
D7	SiG_RTN
A6	N.C
B6	N.C
C6	-12V_AUX
D6	SYSRESET*
A5	GA0*
B5	GA1*
C5	SCL
D5	SDA
A4	+3.3V_AUX
B4	+3.3V_AUX
C4	+3.3V_AUX
D4	+3.3V_AUX
A3	Alert BIT
B3	+12V_AUX
C3	N.C
D3	N.C
A2	N.C
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	N.C
B1	N.C
C1	N.C
D1	Alert BIT

Outline Drawing



Note: Specifications are subject to change without prior notice by the manufacturer.